Synchronizing HSP50214 (PDC) and HSP50215 (PUC)

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Aligning Carrier NCO Frequency

There are a few important points to make about Aligning Carrier NCO Frequency:

1) The phase accumulator in the carrier NCO in the HSP50215 updates at the output clock rate (REFCLK).

2) The phase accumulator in the carrier NCO in the HSP50214 updates when there is a new input sample. This is at the rate that ENIb is asserted and is equal to the input clock rate (CLKIN) when ENIb is tied low.

3) Both NCOs are 32 bits.

4) If REFCLK of HSP50215 equals CLKIN of HSP50214 and ENIb is tied low, then the NCOs will generate the same carrier frequency when loaded with the same 32 bit frequency control word.

5) The carrier frequency will be:

$F_C = F_{CLK} * N / 2^{32}$,

$N = 2^{32} * F_C / F_{CLK}$

F_{CLK} = REFCLK = CLKIN

N = 32 bit control word, twos complement

F_C can be positive or negative to select the upper or lower sideband (spectral inversion).

$-F_{CLK}/2 <= F_C < F_{CLK}/2$

Aligning Resampler NCO Frequency

The input sample rate of the HSP50215 and the output sample rate of the HSP50214 are both controlled by NCOs. Both NCOs are 32 bits. The NCO in the HSP50215 updates at the output sample rate (REFCLK). The NCO in the HSP50214 updates at the output sample rate of the programmable FIR. This rate depends on input mode and decimation. In gated input mode, it is the ENIb assertion rate divided by the decimation in the CIC, halfband filters, and the programmable FIR. In interpolated input mode, it is the CLKIN rate divided by the decimation in the CIC, halfband filters, and the programmable FIR. If ENIb is tied low, it is the same for both modes and equal to the CLKIN rate divided by the decimation in the CIC, halfband filters, and the programmable FIR.

The NCO frequency control words for the HSP50215 (N_{215}) and the HSP50214 (N_{214}) are computed as:

HSP50215: $F_{IN215} = F_{OUT215} * N_{215} / 2^{32}$

HSP50214: $F_{OUT214} = (F_{IN214}/D_{CIC}/D_{HBF}/D_{FIR}) * N_{214} / 2^{32}$

where:

D_{CIC} = decimation of CIC filter;

D_{HBF} = decimation of Half Band filters;

D_{FIR} = decimation of FIR filter.

To make $F_{IN215} = F_{OUT214}$, use the same clock for REFCLK of HSP50215, CLKIN of HSP50214.

* PROCCLK can be asynchronous. There will always be jitter in the HSP50214 output when using the resampler (see below).

$F_{OUT215} * N_{215} / 2^{32} = (F_{IN214} / D_{CIC} / D_{HBF} / D_{FIR}) * N_{214} / 2^{32}$

$N_{215} = N_{214} / D_{CIC} / D_{HBF} / D_{FIR}$; or

$N_{215} = N_{214}$ / (Decimation-to-Resampler)

$N_{214} = N_{215} *$ (Decimation-to-Resampler)

Example:

Assume:

Clock = 52MHz,

$F_{OUT214} = 2 * F_{IN215}$

F_{IN215} = 42kHz, F_{OUT214} = 42kHz

$N_{215} = 0034EED4_{HEX}$,

ACTUAL Frequency = 41.99999944kHz

Assume:

D_{CIC} = 32, D_{HBF} = 16, D_{CIC} = 2 => D_{total} = 1024

$N_{214} = D3BB5030_{HEX}$,

ACTUAL Frequency = 42.000000005kHz

$N_{215} = 00000000001101001110111011010100_b$

$N_{214} = 11010011101110110101000000110000_b$

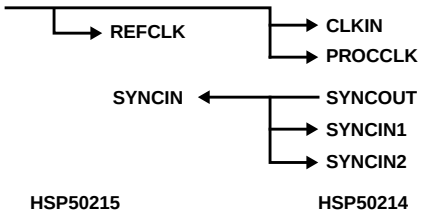
To make the frequencies exactly the same, zero the 10 LSBs of N_{214} to get 0xD3BB5000.

If limited the HSP50214 decimation in the CIC, HBF, and FIR to powers of two, it is possible always to match the frequencies by zeroing LSBs in the N_{214}.

The exact frequency will be set by the accuracy of the NCO in the HSP50215.

Synchronizing Carrier NCO Start-Up /Carrier NCO Phase Alignment

Probably the best way to synchronize the start up of the HSP50215 and HSP50214 is to connect the SYNCOUT of the HSP50214 to the SYNCIN of the HSP50215 and the SYNCIN1 and SYNCIN2, and to use the same clock for all parts.

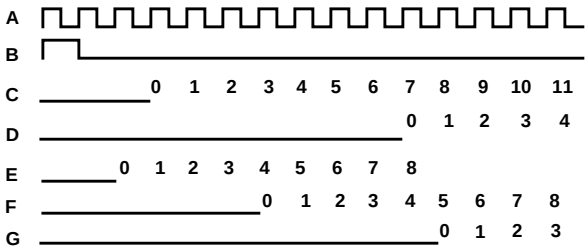


Configure the HSP50214.

Program the HSP50214 to update the carrier NCO on SYNCIN1 (CW0 Bit 20) and to zero the feedback in the phase accumulator on load (CW0 Bit 0). Load the carrier frequency control word into CW3.

Reset the HSP50215. Program all the control registers, setting the HSP50215 for external synchronization (Addr 016, bits 1:0 = 01).

Writing to control word 24 (CW24) generates a one-clock-wide pulse on the SYNCOUT pin. Connecting the parts as shown above and writing to this location will cause both parts to start their NCOs.



A = clock

B = SYNCOUT

C = HSP50215 carrier phase accumulator output samples

D = phase accumulator output sample at HSP50215 output pins

E = HSP50214 carrier phase accumulator output

F = HSP50214 phase accumulator output samples at HSP50214 mixer

G = HSP50215 phase accumulator output samples at HSP50214 mixer

Phase sample 0 is when the phase accumulator's phase = 0. If the output of the HSP50215 is connected to the input of the HSP50214, there will be a phase offset equal to 5 times the NCO phase step to the accumulator step size.

The carrier frequency to the phase accumulator is updated in the HSP50214 on the second clock, following SYNCIN1 going high. The first input sample to be affected by the new frequency will be the sample present at the input 6 clocks after SYNCIN1. (There is a seven clock delay from SYNCIN1 to the mixer through the carrier NCO. There is a one clock delay from the data input to the mixer.)

The HSP50215 detects the rising edge of SYNCIN when external sync polarity is programmed to 0. The carrier NCO will start from a phase of zero on the third clock after the clock period that SYNCIN is active. This sample will be at the output pins seven clocks later.

Offsetting the Phase

The phase of the HSP50214 carrier NCO can be offset in steps of 360/1024 degrees using CW4. This can be used to compensate for the difference in the delay from the zero phase sample of the two phase accumulators to the mixer on the HSP50214.

Frequency Updates

All 32 bits of the HSP50214 frequency control can be updated in a single clock cycle for phase continuous updates. (Set CW0 bit 0 to 0 to disable clearing the phase accumulator feedback on loading.) The updates can be synchronized to the SYNCIN1 signal if desired. Each 16 bits of the 32 bit frequency control on the HSP50215 is updated as it is written, so frequency updates cannot be synchronized between the PDC and PUC.

Synchronizing Resampler NCO Start-Up /Resampler Phase Alignment

The resampler NCO in the HSP50215 starts on SYNCIN (if external SYNC is selected). The resampler NCO in the HSP50214 can be started on SYNCIN2 (CW11 bits 5 and 20). Computing the relative delay is almost impossible because of the many possible configurations of both the HSP50215 and HSP50214. Starting the resamplers together will make the delay fixed and repeatable.

HSP50214 Output Jitter

There is jitter in, when the resampler in the HSP50214 provides output data samples. This is due to the polyphase implementation. On each output of the programmable FIR, the resampler circuitry decides whether there should be an output sample between the last FIR output and the current one. If so, it computes and outputs the sample. If not, it does nothing. This means that output samples are aligned with the FIR output timing, so there will be jitter equal to the FIR output sample period. If the data sample out of the resampler were collected and plotted with even spacing, the output would look clean. If they are reconstructed with a D/A converter and displayed on a spectrum analyzer, there would be additional spurs due to the jitter in, when the samples are provided at the output.